Applicants respectfully assert that claim 25 is novel and patentable over Cho because, for instance, Cho does not disclose or suggest forming a surface sensitive silicon oxide layer over the substrate partially filling the at least one gap, and forming a porous silicon oxide layer on the surface sensitive silicon oxide layer by thermal chemical vapor deposition.

The Examiner alleges that a surface sensitive silicon oxide layer (3) partially fills the gaps. However, Figs. 1A in Cho clearly shows that the layer (3) completely, not partially, fills the gaps.

For at least the foregoing reasons, claim 25 and claim 26 depending therefrom, are patentable.

Claims 1-9 and 23-24

Claims 1, 2, 4-7, 9, and 23-24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho in view of Kwok.

Applicants respectfully submit that independent claim 1 is patentable over Cho and Kwok because, for instance, they do not disclose or suggest forming a porous silicon oxide layer on the surface sensitive silicon oxide layer, wherein the surface sensitive silicon oxide layer has a wet etch rate of greater than about 6000 Å/min.

Although Kwok discloses a wet etch rate of much greater than 10,000 Å/min for a high ozone film on thermal oxide, it does not teach or suggest forming a porous silicon oxide layer over a surface sensitive silicon oxide layer having a wet etch rate of greater than about 6000 Å/min. Moreover, nothing in Kwok or Cho provides the motivation to modify Cho by forming the insulating layer (3) at a wet etch rate of greater than about 6000 Å/min. Applicants respectfully submit that the Examiner's combination of Cho and Kwok benefits from the exercise of hindsight.

In addition, Applicants note that the wet etch rate range is a critical range that produces unexpected results. In *In re Aller*, 105 U.S.P.Q. 233, 235 (C.C.P.A. 1955), the court stated that if the recited ranges were shown to be "critical" ranges that produced a new and unexpected result, then the claimed process would be patentable. When the specification describes a range that is not merely preferred but necessary, such a range is

critical. *In re Waymouth*, 182 U.S.P.Q. 290, 293 (C.C.P.A. 1974). *Waymouth* involved a high pressure discharge lamp that produced white light from a mixture of halogen and mercury atoms present in a specified ratio of a range from 0.08 to 0.75. *Id.* at 291. The court concluded that the claimed range was a critical range that produced unexpected results even though the prior art disclosed a range of possible ratios that enveloped the claimed range. *Id.* at 293. In reversing the rejection of the claims, the court noted that it was the applicant who had discovered that any relationship existed at all between the halogen atom to mercury atom ratio and the intensity of white light emission. *Id.*

In the present application, the specification itself has established that the recited wet etch rate range is critical. The range of greater than about 6000 Å/min provides a surface sensitive silicon oxide layer. A porous silicon oxide layer is then deposited over the surface sensitive underlayer using a thermal CVD process. The porous silicon oxide layer is significantly more porous than a similar layer deposited over non-surface sensitive layers (page 18, lines 3-8).

The inventors discovered it was critical to provide a surface sensitive layer having a wet etch rate of greater than about 6000 Å/min to form the desirable porous silicon oxide layer on the surface sensitive layer. In one example, the density is reduced from 2.1-2.2 g/cm^3 to 1.2-1.7 g/cm^3 (page 18, lines 8-11), and the dielectric constant is reduced from about 4.2-4.4 to about 2.9-3.2 (page 18, lines 12-15). Therefore, the difference achieved by the present process at the critical wet etch rate range is a difference in kind, rather than in degree. Accordingly, claim 1 is patentable over Cho and Kwok.

Claims 2, 4-7, 9, and 23-24 depend from claim 1, and are submitted to be patentable as reciting additional features of the invention as well as by being dependent from allowable claim 1. For example, claim 2 recites that the porous silicon oxide layer has a carbon content of at least 5 atomic percent. Claim 4 recites that the surface sensitive silicon oxide layer is deposited from a plasma enhanced CVD reaction of TEOS and oxygen. Claim 23 recites that the substrate includes at least one gap, and the surface sensitive silicon oxide layer partially fills the at least one gap. Claim 24 recites that the

porous silicon oxide layer fills the at least one gap. These features are absent from the cited references.

For at least the foregoing reasons, claim 1 and claims 2, 4-7, 9, and 23-24 depending therefrom are novel and patentable over Cho and Kwok.

Claims 3 and 8 depend from claim 1, and stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho in view of Kwok and Lan (USP 6,180,507). Lan is cited for allegedly disclosing that the porous silicon oxide layer has a dielectric constant lower than that of a conventional silicon oxide layer.

Applicants note that Lan fails to cure the deficiencies of Cho and Kwok because, for instance, Lan does not teach or suggest forming a porous silicon oxide layer on the surface sensitive silicon oxide layer, wherein the surface sensitive silicon oxide layer has a wet etch rate of greater than about 6000 Å/min, as recited in claim 1 from which claims 3 and 8 depend. Therefore, claims 3 and 8 are patentable over Cho, Kwok, and Lan.

Claims 10-19 and 21-22

Claims 10-19 and 21-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cho and Kwok in view of Lan.

Applicants respectfully assert that independent claim 10 is patentable over Cho, Kwok, and Lan because, for instance, they do not teach or suggest depositing a plasma enhanced CVD silicon oxide layer over a plurality of conductive lines, and depositing a thermal silicon oxide layer over the plasma enhanced CVD silicon oxide layer. These references also fail to disclose or suggest that the thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent.

The Examiner concedes that Cho fails to teach forming a plasma-enhanced CVD silicon oxide layer, but alleges that it would have been obvious to modify Cho in view of Kwok to form a plasma-enhanced CVD silicon oxide layer. Cho discloses varying TEOS flow rates while forming intermetallic insulating layers, and does not mention plasma at all. Kwok is directed to the study of surface related phenomena of O_3-

TEOS SACVD films on different types of plasma-enhanced CVD oxides. Cho and Kwok relate to different processes and solve different problems. The references do not provide any teaching whereby the combination would have been obvious. Thus, Applicants believe the Examiner has engaged in the impermissible hindsight reconstruction of the claimed invention in this regard.

Furthermore, the cited references do not disclose or suggest that the thermal silicon oxide layer has a dielectric constant of about 3.2 or less and a carbon content of at least about 5 atomic percent. The Examiner alleges that it is "inherent that an insulating film formed by a carbon containing silane, Tetraethylorthoxisilicate gas (TEOS) contains a carbon content of at least 5 atomic %." This assertion is speculative and baseless. "Prior art SACVD O_3/TEOS layers generally have a carbon content of between 2-3 at.%. The porous SACVD O_3/TEOS layer of the present invention, however, has a significantly higher amount of carbon, at least 5 at.%, incorporated into the layer." Page 18, lines 30-33.

Claims 11-19 and 21-22 depend from claim 10, and recite additional features not taught or suggested in the references. For example, claim 18 recites that the plasma enhanced and thermal CVD silicon oxide layers are deposited in an in situ process. Claim 21 recites that the plasma enhanced CVD silicon oxide layer partially fills gaps between the plurality of conductive lines. Claim 22 recites that the thermal silicon oxide layer fills the gaps between the plurality of conductive lines.

For at least the foregoing reasons, claim 10 and claims 11-19 and 21-22 depending therefrom are patentable over Cho, Kwok, and Lan.

///

///

///

///

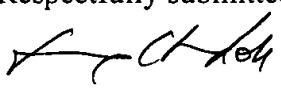
///

///

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is urged. If the Examiner believes a telephone conference would aid in the prosecution of this case in any way, please call the undersigned at 650-326-2400.

Respectfully submitted,



Chun-Pok Leung
Reg. No. 41,405

TOWNSEND and TOWNSEND and CREW LLP
Tel: 650-326-2400
Fax: 415-576-0300
RL:rl
PA 3279333 v1

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 17, TABLE 2, please change "500 Å/min" to --5500 Å/min--.

Page 17, please delete footnotes 1 and 2.

Page 17, lines 2-7, please amend the paragraph as follows:

From Table 2, if the underlayer is thermal oxide then the deposition rate is lower, the wet etch rate is significantly higher, the surface roughness worse, and the stress hysteresis, in a room temperature to 360°C heat cycle, is higher than an underlayer of bare silicon. With PE-TEOS as an underlayer, the effects were in between, with the wet etch rate, surface roughness, and stress hysteresis being relatively close to the thermal oxide values. In Table 2, the bare silicon values and thermal oxide values are from Table IV of the Kwok paper, and the PE-TEOS values are estimated from the graphs in Figs. 1-6 of the Kwok paper.

IN THE CLAIMS:

Please amend claims 1 and 19 as follows.

1. (Twice amended) A method for forming an insulation layer over a substrate, the method comprising:

forming a surface sensitive silicon oxide layer over the substrate; and

forming a porous silicon oxide layer on the surface sensitive silicon oxide layer by thermal chemical vapor deposition, wherein said porous silicon oxide layer is deposited at a temperature of about 400°C or less;

wherein the **[porous]** surface sensitive silicon oxide layer has a wet etch rate of greater than about 6000 Å/min.

19. (Amended) The process of claim 10 wherein said **[porous]** silicon oxide layer is deposited using an SACVD process at a pressure of between 100-700 Torr.